26.2 A 512kB Embedded Phase Change Memory with 416kB/s Write Throughput at 100μA Cell Write Current

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Small inexpensive IC chips operated with very low power consumption are key devices in the ubiquitous era [1]. The embedded ROM modules of these devices must be re-writable for data collection and configuration setting in the field. In addition, these modules also require high density to have a communication function. Our previously developed phase change memory (PCM) cell consists of a Ta_2O_5 interfacial layer and features low voltage (1.5V) and low current (100μA) write operation [2]. This performance enables memory array fabrication using a standard CMOS process and dramatically reduces the embedded ROM module size by removing high-voltage-operated components. Thus, our device is suitable for ubiquitous applications. On the other hand, the readout current is restricted to less than 60μA to avoid read disturbance [3]. Moreover, the current of the high resistive state is down to the order of nanoamperes. The enhancement of the read speed and the establishment of the test scheme of such a small readout current cell are indispensable for implementing our PCM cell.

In this paper, we describe an experimental 512kB embedded PCM module with current-saving architecture. It features a sense amplifier prefetch serial write scheme combined with a two-step set method, a charge-transfer direct-sense scheme, and an array stand-by voltage control scheme for cell current measurement in test mode. These techniques enable our PCM module to perform write operations at 416kB/sec with a cell current of 100μA and 9.9ns read access time in a memory array (Fig. 26.2.1).

To reduce the current consumption, a serial write mode is indispensable for the PCM [4]. In this mode, a single cell performs the write operation, while 16b data is simultaneously input into the PCM module. To apply the parallel-serial conversion to the memory array, we introduce a sense-amplifier-prefetch serial write scheme. Figure 26.2.2 shows the scheme, which uses 16 sense amplifiers (SA0-SA15) and write circuits (WC0-WC15), arranged on a 128kb memory array. Programming data are temporarily stored in these sense amplifiers in response to 16 input/output lines (I/O0-I/O15). Afterwards, mask signals (MSKB0-MSKB15) activate these write circuits one by one and the data are serially written into respective memory cells.

The write time of a single cell must be reduced to suppress the total time of the serial write operation. To reduce the set time, we introduce a two-step set method that is a modified version of a staircase-down set [5] (Fig. 26.2.3). The two-step pulse applied to a bit-line consists of two phases. In the first phase, the pulse shape is the same as that under the reset operation. In the second phase the bit-line voltage is lowered.

We evaluate the effectiveness of this method by using a test cell. The set time is reduced from 1μs to 300ns by using this scheme. The operation window of the set bitline voltage,V_{BS}, on an *x*-axis and the word line voltage, V_{WL}, on a *y*-axis was more than 0.3V. This value is large enough to tolerate the fluctuation of internal voltages.

Low power, not only for write operations, but also for read operations, is an important function for ubiquitous devices. To prevent read disturbance, the readout current of the set state cell is suppressed to 4μA (= 0.4V/100kΩ) in the worst case. Conventional charge-transfer sensing and differential-input-current sensing speed up read operations, but these schemes consume DC currents in the voltage regulator or the sense amplifier [6,7]. Therefore, we develop a charge-transfer direct sense scheme to achieve high-speed and low-power operation, as shown in Fig. 26.2.4.

In this scheme, a direct preamplifier is composed of three pair MOS transistors: (PA, PA'), (PB, PB'), and (NA, NA'). The first pair precharges output nodes SAINT, SAINB to the V_{DD} supply voltage of 1.5V. Bitlines are precharged to a read bitline voltage V_{BR} of 0.5V. When the second transistor pair is activated by the third pair, the output nodes are discharged.

Since the readout voltage developed on bitlines are input to both gate and drain nodes of the second pair transistors (PB, PB'), the difference of driving capabilities between these pair transistors is increased. In addition, input/output nodes of the preamplifier and a second stage amplifier are biased to rail-to-rail voltages, these amplifiers perform without an additional timing slot. Therefore, as shown in Fig. 26.2.5, it takes less than 9.9ns to perform the read operation from wordline activation to the completion of data-latch. This result is shorter than our design target for read access time of 14ns in the memory array, and shows the feasibility of 20ns access in the memory module. The scheme has good robustness against V_t fluctuation induced by process variation. The current draw in the sense amplifier is suppressed to the same level as that of a conventional sense latch, 280μA, under simultaneous 16b read operation.

The design for testability is an essential issue for the mass production of emerging memories. Since the reset resistance of our PCM cell is from 1MΩ to several ten megaohms, its readout current is in the order of nanoamperes. Thus, the measurement accuracy of this current depends on the leakage current on the current path through a test pad (T-PAD) to the memory cell, as shown in Fig. 26.2.6. To suppress this current, we develop an array standby voltage control scheme. Voltage switches selectively supply a ground voltage, V_{SS}, to source lines of a 64:1 mux and a memory array in user operation mode, and a leakage current reduction voltage, V_{LCR}, in test mode. This additional voltage is typically equal to the read bitline voltage, V_{BR}. In the 64:1 mux in test mode, leakage currents from a common bitline (CBL0E) to unselected bitlines (BL1 to BL63) are suppressed. Moreover, in unselected cells on the selected bitline (BL0), leakage currents are also reduced.

In the module, the total gate width of MOS transistors generating leakage currents on the cell current path is 500μm, and the total leakage current is estimated to be 1.5nA (3pA/μm in the typical condition). Assuming a measurement accuracy of 10%, the current measured at the test pad up to 15nA is allowed. This results in the cell resistance of 33MΩ (= 0.5V/15nA). If a V_t reduction of 100mV is caused by process variation and the leakage current increases to 15nA, the leakage current is suppressed more than one order of magnitude by using the proposed scheme. Therefore, the upper limit of measured resistance is improved from 3MΩ to 33MΩ.

We have developed a current-saving architecture for an embedded PCM. The sense-amplifier-prefetch serial-write scheme featuring a two-step set method achieves 416kB/sec write throughput at the cell write current consumption of 100μA. The charge-transfer direct sense scheme reduces the read access time to 9.9ns in the memory array. The array standby voltage control scheme suppresses leakage currents and enlarges the measured resistance range of our PCM cell to 33MΩ. Figure 26.2.7 shows the die micrograph of the chip fabricated in a 0.13μm 1.5V CMOS process.

References:

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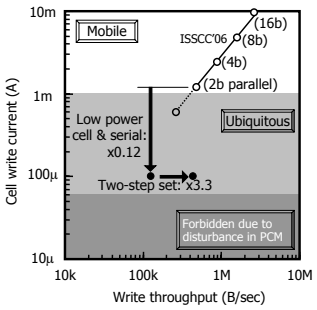

Process		4-Cu, 0.13μm/1.5V CMOS
Cell size		0.68×1.04μm²
Write	Cell current	100μA/bit
	Set time	300ns/bit
	Throughput	416kB/sec (serial)
Read (x16)	Cell current	4μA/bit (worst)
	SA current	280μA (average)
	Access time	9.9ns (in 128kb array)
Module size		2,600×4,000μm²

Figure 26.2.1: Performance of embedded PCM for ubiquitous era.

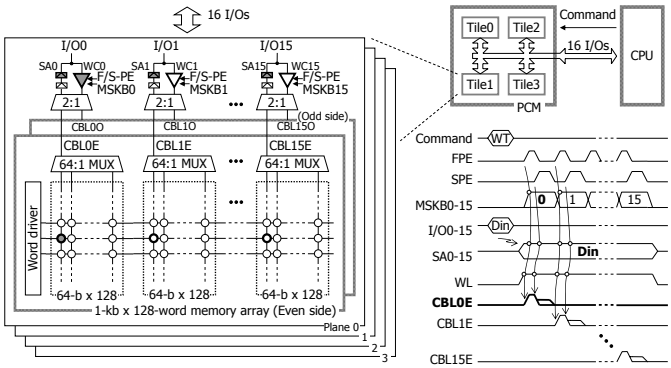

Figure 26.2.2: Sense-amplifier-prefetch serial write scheme.

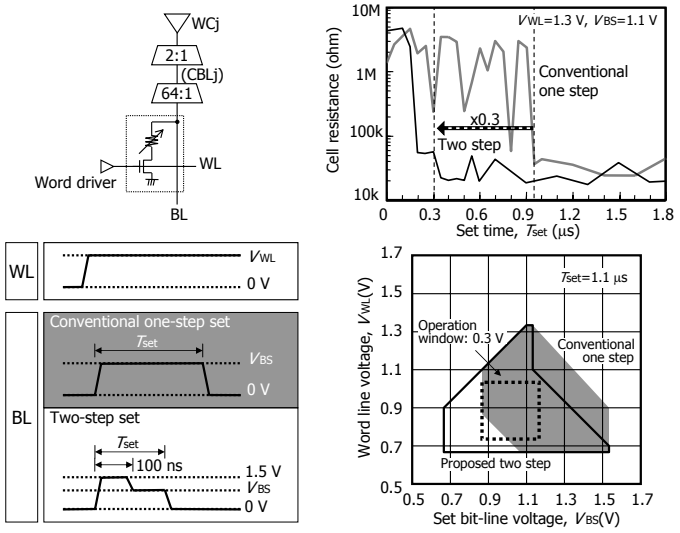

Figure 26.2.3: Two-step set method.

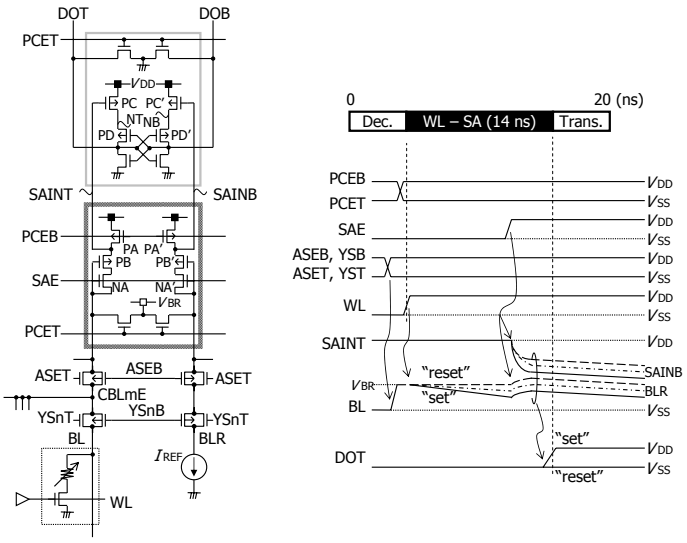

Figure 26.2.4: Charge-transfer direct-sense scheme.

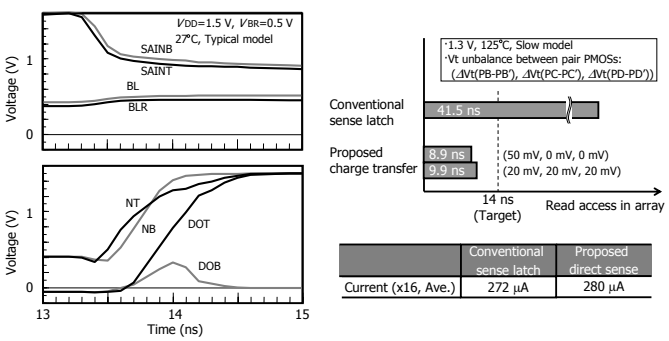

Figure 26.2.5: Simulated waveforms and performance of proposed scheme.

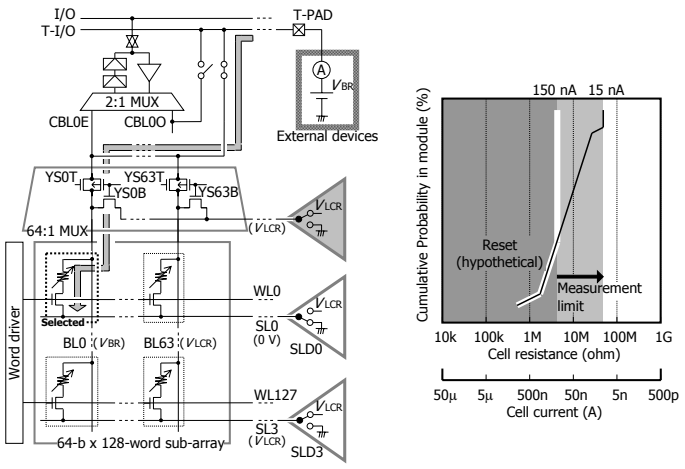

Figure 26.2.6: Array standby voltage control scheme for cell current measurement in test mode.

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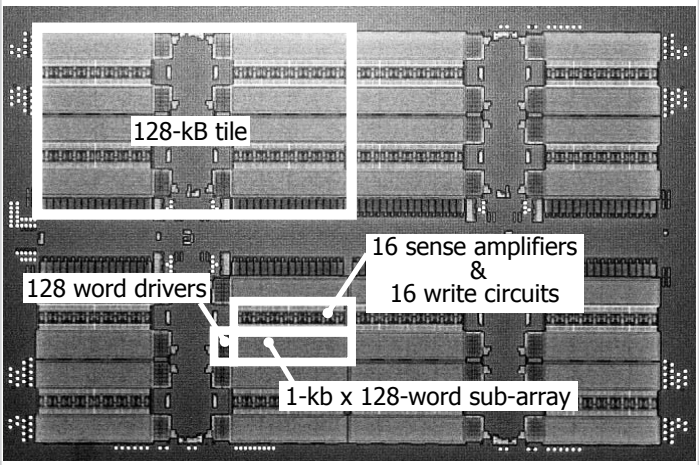

Figure 26.2.7: Die micrograph of experimental 512kB embedded PCM.

